



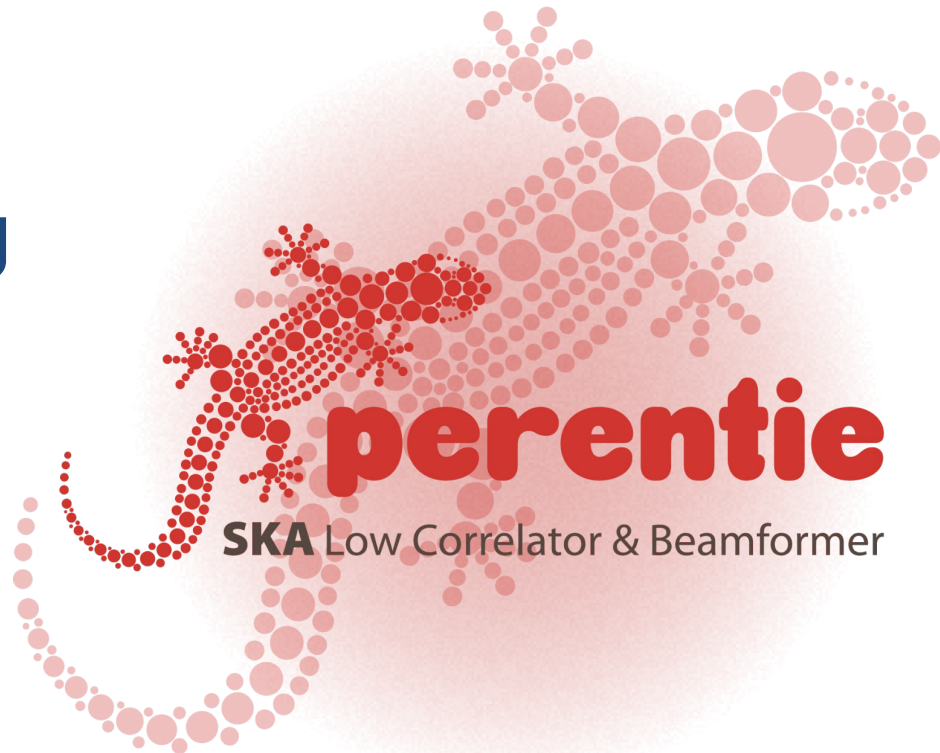
Low.CBF Modelling

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Overview



What is low.CBF ?

How will it work ?

What are the challenges ?

Where are we at ?

The Low Correlator and Beamformer

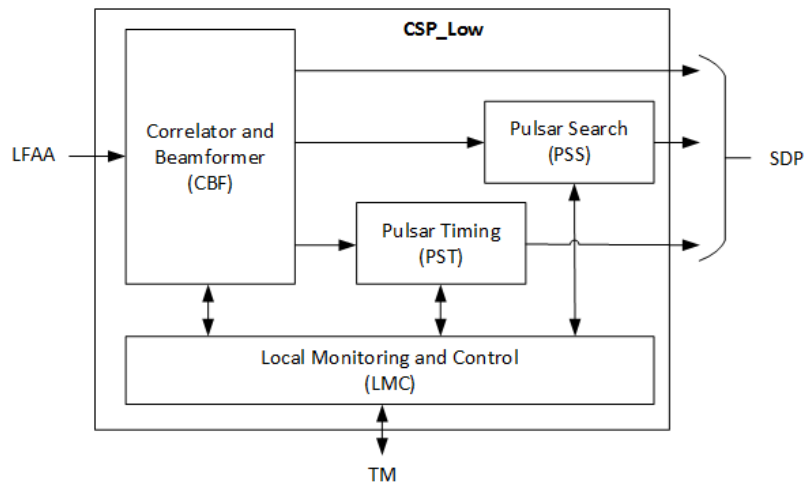


Challenges

Cost/Power/Space/Cooling/Comms

Goals

- **Reduce Risk by developing and testing key functions**
 - **ITF**
 - **Modelling algorithms and interfaces**
 - **Firmware and Software**

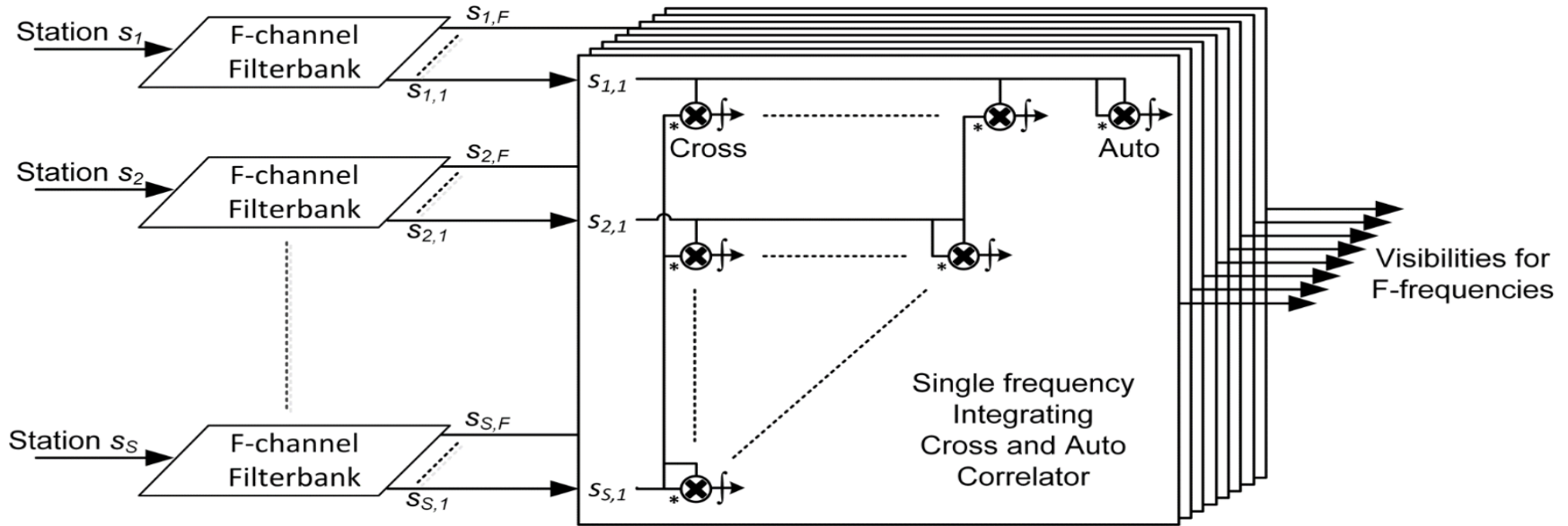


Correlator



- **Correlator operates on fine channels 226 Hz wide.**
- **Total of 300 MHz/226 Hz = 1.3 million**
- **Need to correlate each station with every other station**
- **Each FPGA processes data for all stations for a small number of fine channels.**

FX Correlator

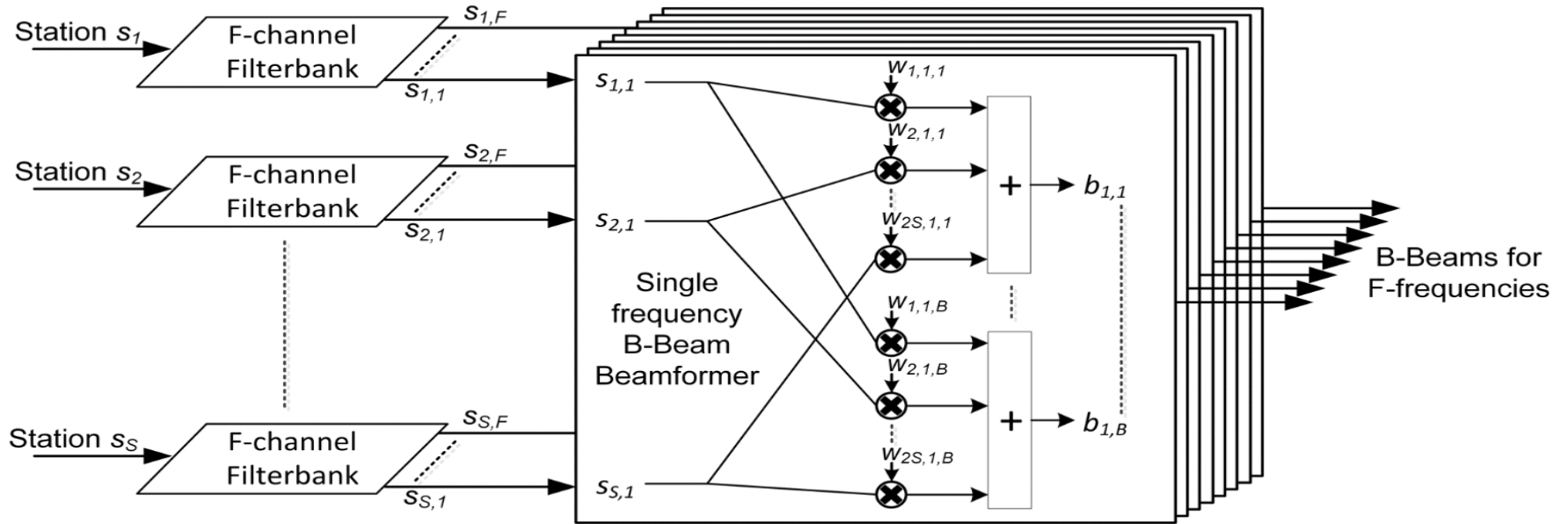


Beamforming

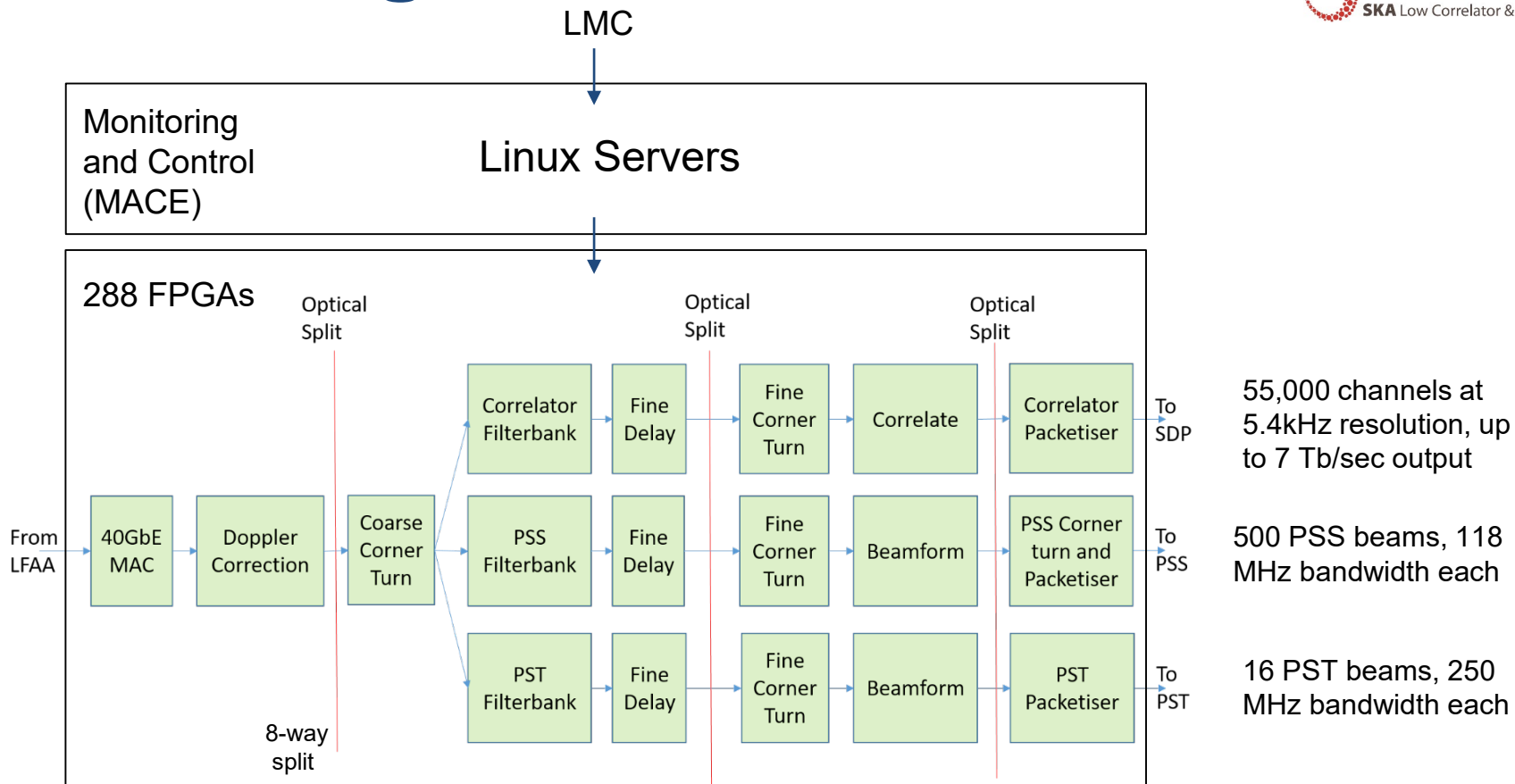


- **Each Beam is a weighted sum of appropriately delayed data from all stations.**
- **PSS**
 - 500 beams,
 - 20736 x 14 KHz fine channels
- **PST**
 - 16 beams
 - 82944 x 3.6 KHz fine channels
- **Both cases process data from all stations**
 - But each processing element can do a subset of fine channels.

Beamformer Data Flow



Processing Overview

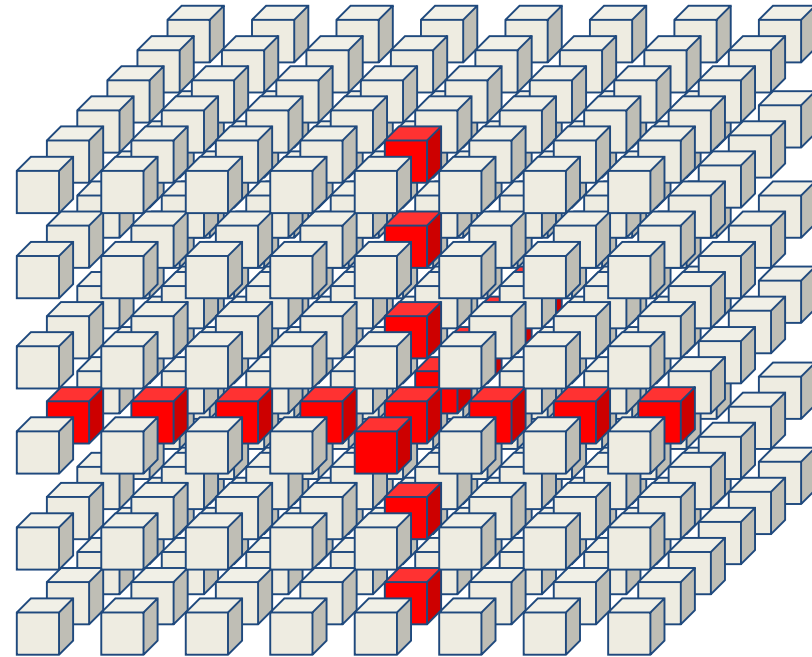


Full Scale System

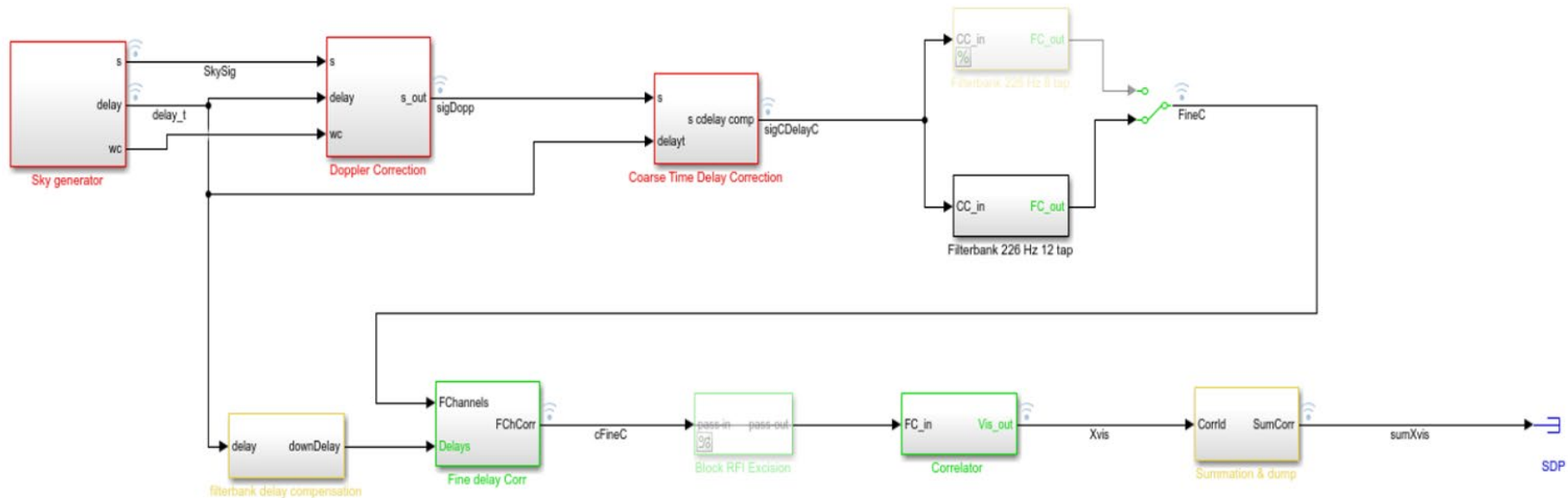


288 FPGAs arranged in an array, 8x6x6

- **Lots of communications - see Will's talk**
 - **All optical, total per FPGA of about 1Tb/s**
- **Total input and output data rates both over 5 Terabits/sec**
 - **E.g. LFAA 11 Gbit/sec x 512 stations = 5.6 Tbit/sec**
- **Total computation in the realm of 2 Peta ops/second**
- **Total power about 50 kW**



“Golden” model



Software modelling

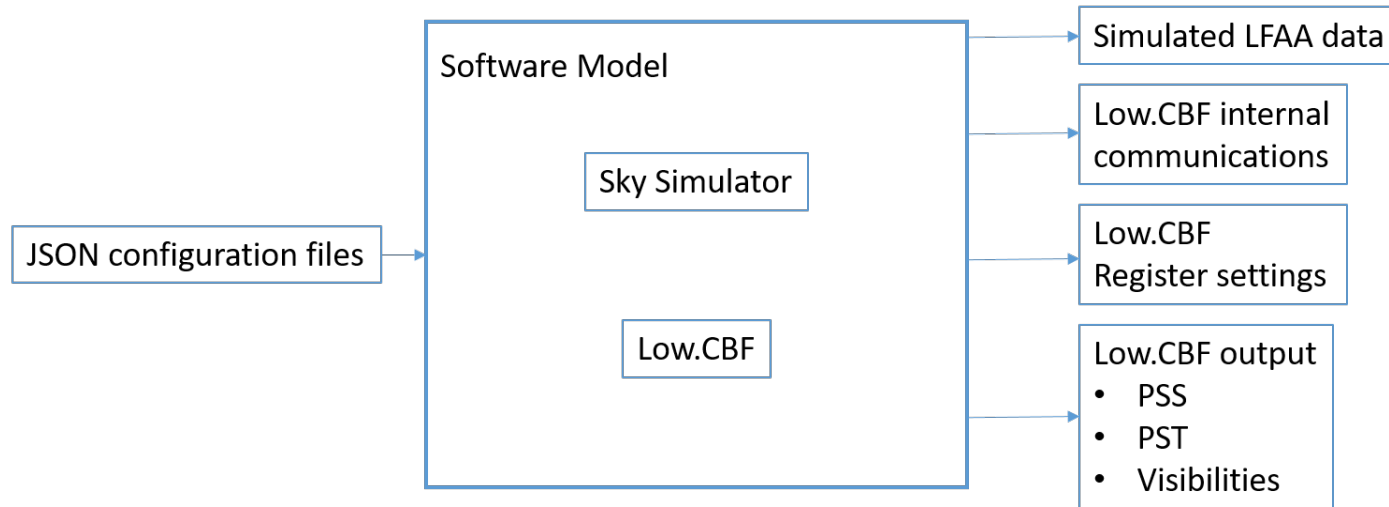


System Modelling Goals

- **Flexible**
 - **Used for firmware module verification**
 - **Used for stimulus/checking in the ITF**
 - **Used to verify register configuration**
 - **Many configurations possible**
- **Realistic**
 - **Model Configuration to match the TM/LMC parameters in the ICDs**
 - **Top level parameter specifications for a run in json files.**
- **Verification at multiple levels**
 - **low.CBF Algorithms**
 - **Generate expected input and output of firmware modules**
 - **Generate firmware register settings**

More Modelling

- **Model Configuration specified using JSON - matches with ICDs**
- **Able to limit processing to a small number of processing elements and frequency bands**
- **Efficient formats for raw data files**
 - **22 Gb/s of traffic per LFAA input !**



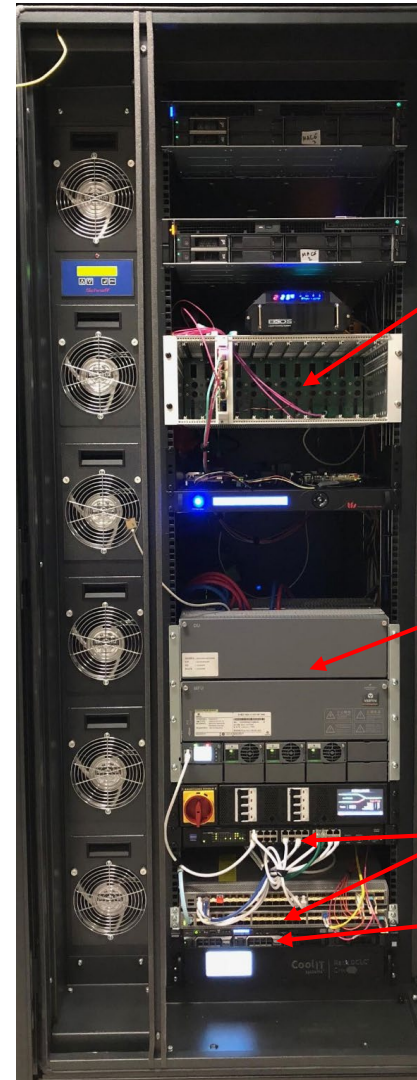
Expected FPGA Utilisation



Resource	Available (Virtex Ultrascale+ VU37P)	Expected Utilisation
Multipliers	9024	6000
6 input Look up tables	1.2 million	600,000
On Chip Memory	40 Mbytes	20 Mbytes
High Bandwidth Memory	8 Gbytes	8 Gbytes
DDR4	8 Gbytes (on board)	TBD
High Speed Serial links	96 GTY transceivers, can run up to 32 Gbit/sec	100 GbE (4 GTYs) 40 GbE (4 GTYs) 10 GbE (1 GTY) 24 x 25 Gb (24 GTYs)

Progress to Date

- Send simulated LFAA packets to the ITF.
- Key firmware modules underway
 - Correlator
 - Filterbanks
 - Ethernet Comms
- More on some of these things later...



Gemini Subrack

48VAC-DC

Network Switch

MACE Server

Still to do...



Lots of things still to do...

- Testing of HBM part.
- Finish software model.
- More firmware to write, and integrate.
- Running all communication links.

Questions / Discussion?

Thank-you!