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COMPUTING FOR SKA

ASIC FOR SKA - SKASIC

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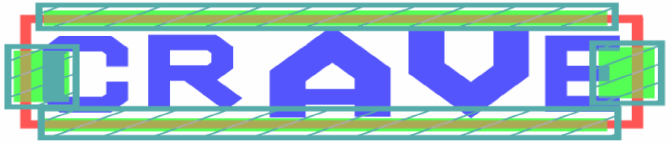

COMPUTING FOR SKA

Massey University Overview

- Massey University is the 2nd largest university in New Zealand
- The School of Engineering and Advanced Technology (including Computer Science) have over 70 academic staff, along with over 100 Ph.D. students.
- High PBRF score in Engineering and Technology
- A leader in Electronic and Computer Engineering Research

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***Center for Research in Analog & VLSI microsystem dEsign (CRAVE)**
***HASAN VLSI GROUP**

*Only Center for Integrated Circuit/VLSI/ASIC design in New Zealand

*Nearly 100 conference and 60 Journal publications in IC/VLSI/ASIC design

*Microchip design experience using Cadence, Mentor Graphics, Synopsys, Tanner Tools

*Chip Fabrication experience through IBM, TSMC, Agilent and AMS silicon foundries

*Experience in Analog, Digital, Radio-Frequency, Mixed-Signal, ASIC, SOC, MEMS. Node-size down to 28 nm CMOS

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ASIC DESIGN

- IC Design for a Specific Application

PURPOSE

- Reduce power dissipation
- Reduce hardware cost and size
- Achieve higher processing speed
- Reduce memory and bus/bandwidth bottle-necks
- Improve overall system reliability

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ASIC DESIGN

INFRASTRUCTURE REQUIREMENT

- Foundry Access - often through third parties, Global Foundries (mostly IBM processes), ST Microelectronics, TSMC – often requiring 3-tier NDAs
- Design Tool Access – Cadence, Mentor Graphics, Synopsys - NDAs
- Workforce trained in circuit and system design
- Experience in packaging design and/or package selection
- Experience in Fab design submission and prototype testing
- Micro-probing using probe pads and Testing Facilities

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ASIC DESIGN

ASIC DESIGN METHODOLOGY

- Architecture Development and functional/VHDL simulation
- Standard Cell/ Full Custom Design (often cell library including SRAM, DRAM, I/O available from foundry)
- Synthesis from RTL using standard cells/custom cells
- SPR (Placement and routing) to optimize chip-size including power supply and global clock routing
- Logic verification and Timing analysis (critical path analysis)
- Calibre DRC, Parasitic extraction and LVS (layout vs. schematic)
- Packaging design/selection

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ASIC DESIGN

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- Various components in CSP and DISH work packages
- For example, Cross-correlator for CSP and Beam-former for DISH
- Has been investigated for DISH TDBF PDR
- Is being investigated for Wavefront array correlator for CSP and Pulsar search
- Primary goal – drastic reduction of power dissipation (reduce running cost)
- Secondary goal – low NRE and unit production/manufacturing cost

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ASIC DESIGN

ASIC for TDBF

- 28nm GF SLP, 28nm GF HPP or 28nm ST Microelectronics FDSOI CMOS
- ARM standard cell library/ ST microelectronics cell library
- 15 G/s SERDES IP
- Power: 20W/chip (@ 1.2 GHz)
- size: 11mm x 11mm
- cost: $230 @ 10K quantity
- Package: Flip-chip BGA

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ASIC DESIGN compared to FPGA

- Unlike FPGA ASIC design requires considerable design platform, infrastructure and FAB connections.
- ASIC unit cost is usually cheaper for higher volume, upwards 100K volume
- For the same process technology ASIC will almost certainly have lower running cost
- ASIC will in most cases ease I/O as compared to FPGA
- Operating speed supported is likely to be higher compare to FPGA
- ASIC has high NRE compared to FPGA, but lower NRE in an university VLSI design environment

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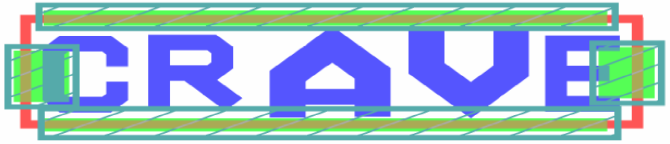

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Thank You!