MASSEY UNIVERSITY

An Architecture for the X-Part of a Large FX Correlator using Two-Accumulator CMACs

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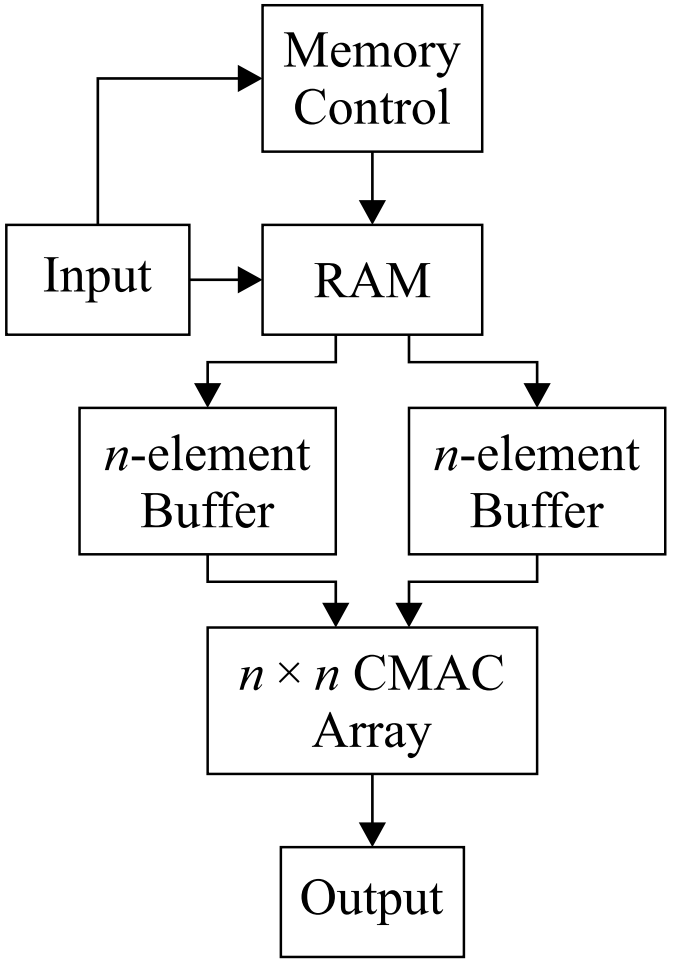
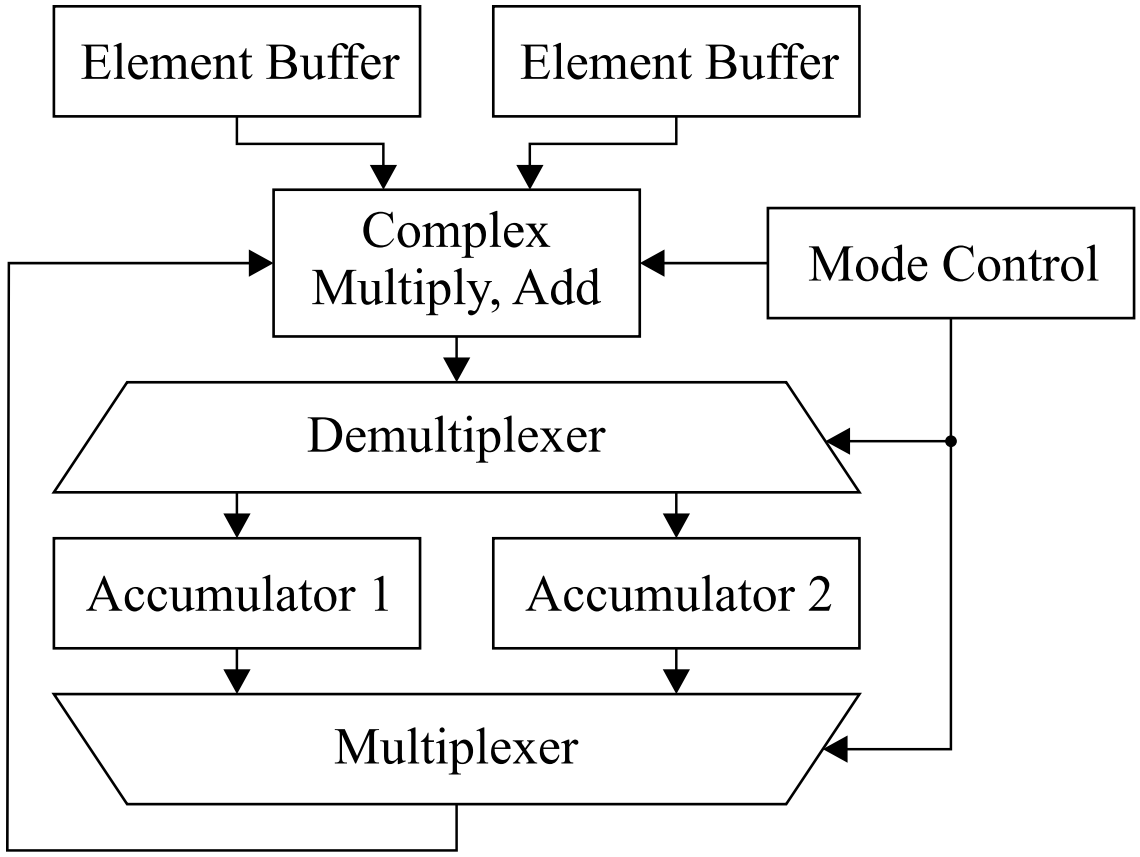
Original Architecture

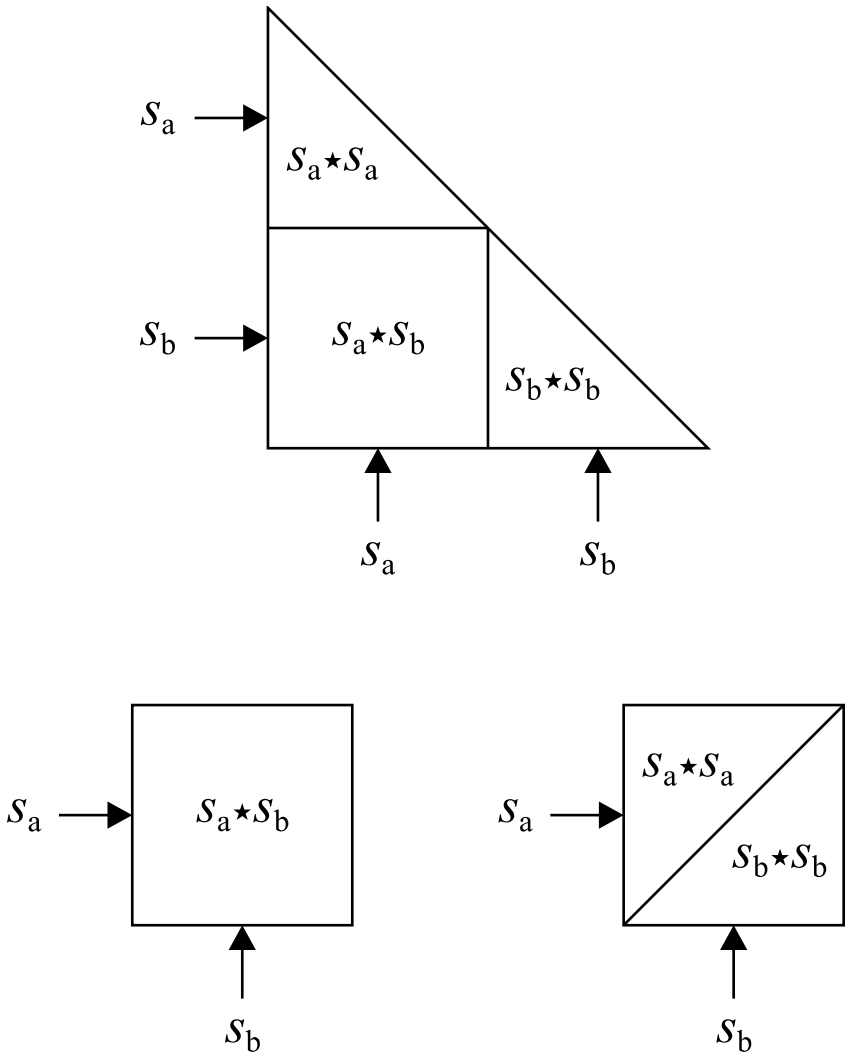


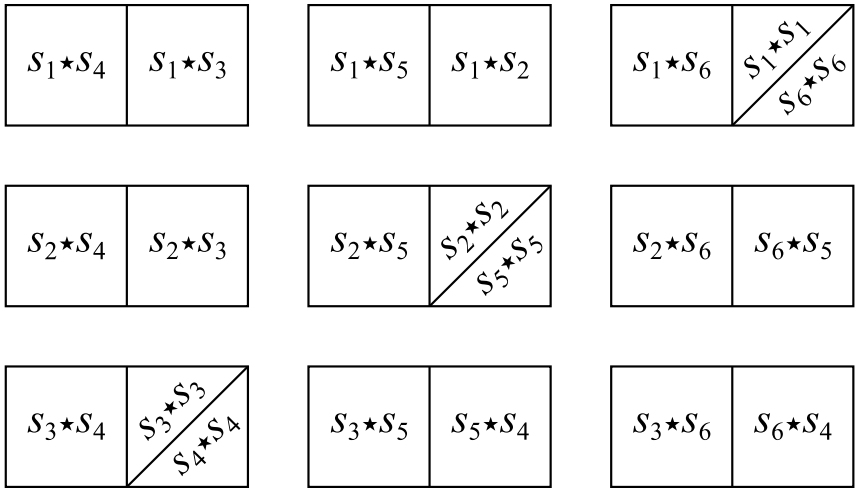
- Requires a corner-turner
- The memory is loaded with samples for all $2N$ signals for a portion of frequency channels
- Input signals are split into w sets of n signals
- Every set is correlated with all sets
- One integration produced by the CMAC array is called a sub-integration

Original Architecture Inefficiencies

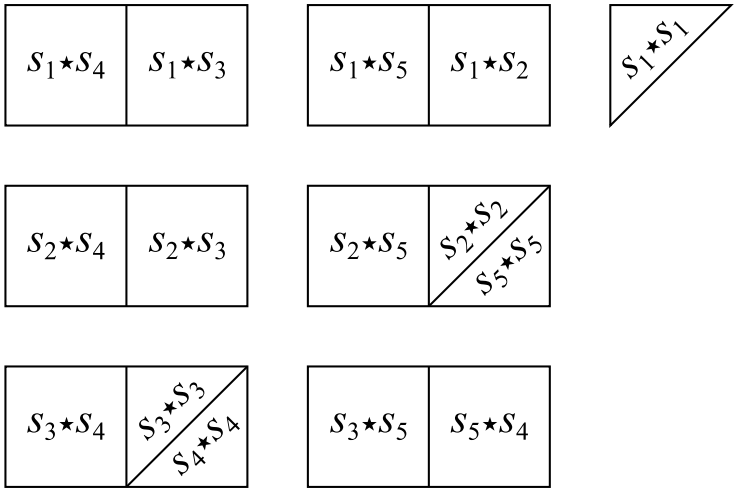
- Every sample is read w times from the memory because it is used in w sub-integrations
- CMAC rate is half the memory rate. CMACs are capable of much higher rates.
- Maximum memory rate (usually) limits the overall processing bandwidth


Element Buffer
Element Buffer
Complex
Multiply, Add
Mode Control
Demultiplexer
Accumulator 1
Accumulator 2
Multiplexer

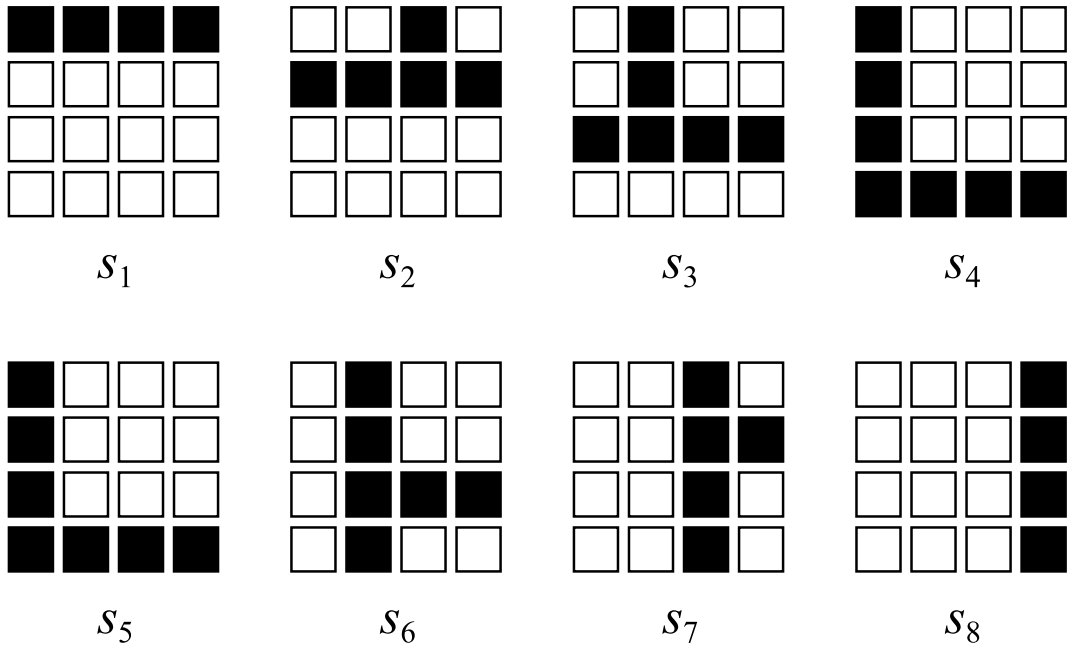

S_a
$S_a \star S_a$
S_b
$S_a \star S_b$
$S_b \star S_b$
S_a
S_b
S_a
$S_a \star S_b$
S_b
S_a
$S_a \star S_a$
$S_b \star S_b$
S_b


$s_1 \star s_4$
$s_1 \star s_3$
$s_1 \star s_5$
$s_1 \star s_2$
$s_1 \star s_6$
$s_1 \star s_1$
$s_6 \star s_6$
$s_2 \star s_4$
$s_2 \star s_3$
$s_2 \star s_5$
$s_2 \star s_2$
$s_5 \star s_5$
$s_2 \star s_6$
$s_6 \star s_5$
$s_3 \star s_4$
$s_3 \star s_3$
$s_4 \star s_4$
$s_3 \star s_5$
$s_5 \star s_4$
$s_3 \star s_6$
$s_6 \star s_4$

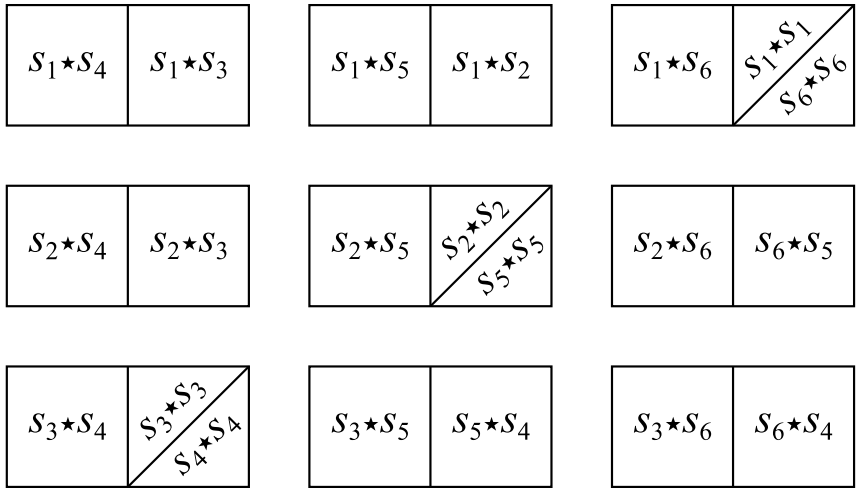
$w = 6$


$s_1 \star s_4$
$s_1 \star s_3$
$s_1 \star s_5$
$s_1 \star s_2$
$s_1 \star s_1$
$s_2 \star s_4$
$s_2 \star s_3$
$s_2 \star s_5$
$s_2 \star s_2$
$s_5 \star s_5$
$s_3 \star s_4$
$s_3 \star s_3$
$s_4 \star s_4$
$s_3 \star s_5$
$s_5 \star s_4$

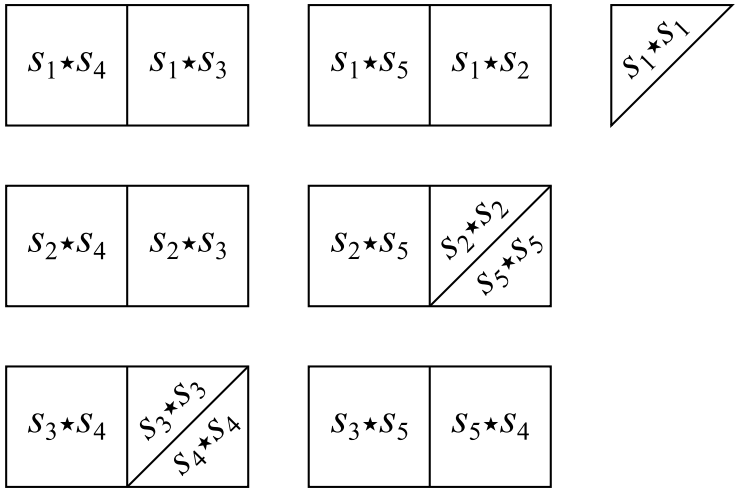
$w = 5$



The number of pairs each signal is used in varies from $w/2$ to $w - 1$.



$w = 6$



$w = 5$

Per $2N$ samples:

- When w is even, total read/write sample rate is

$$nw^2\left(\frac{3}{4} + \frac{1}{2w}\right)$$

- When w is odd, the rate is

$$nw^2\left(\frac{3}{4} + \frac{1}{2w} + \frac{3}{4w^2}\right)$$

- The rate for the original architecture is

$$nw^2\left(1 + \frac{1}{w}\right)$$

- Ratios of memory rates to the original rate are

$$R_{\text{even}} = \frac{3/4 + 1/(2w)}{1 + 1/w}$$

$$R_{\text{odd}} = \frac{3/4 + 1/(2w) + 3/(4w^2)}{1 + 1/w}$$

Equal Processing Bandwidth Example

$$2N = 240$$

Original Architecture

- $n = 48$
- $w = 5$

Per $2N$ samples:

- 30 memory cycles
- 1440 samples accessed

Hardware:

- 2304 CMUL+CADD
- 4608 accumulators

Improved Architecture

- $n = 40$
- $w = 6$

Per $2N$ samples:

- 30 memory cycles
- 1200 samples accessed

Hardware:

- 1600 CMUL+CADD
- 6400 accumulators

-704 CMAC processing circuits and $+1792$ accumulators