CSIRO

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TE WĀNANGA ARONUI O TAMAKI MAKAU RAU

ASTRON

Cramming the H into HBM

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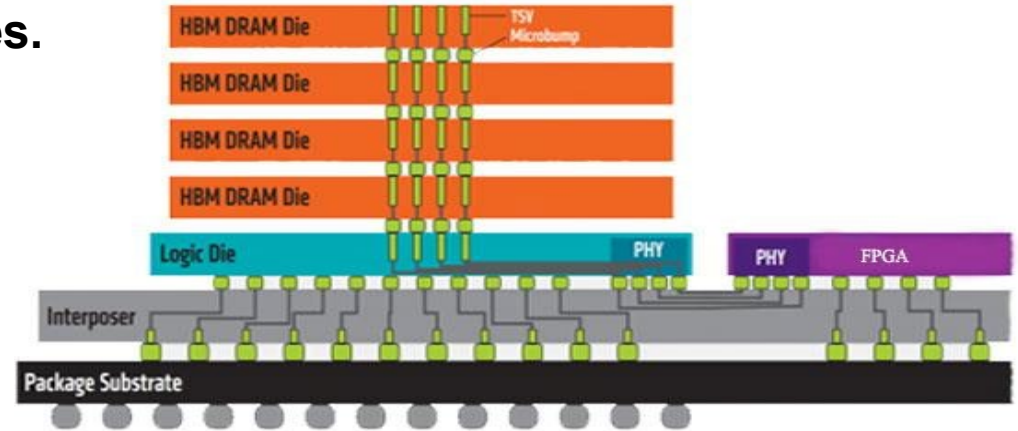
High Bandwidth Memory (HBM)

- HBM is a new type of memory chip.
- Vertically stacked memory chips interconnected by Through Silicon Vias (TSV).
- Low power consumption.
- Ultra wide communication lanes.
- Faster speed.
- Less Area.



Stacked Silicon Interconnect (SSI)

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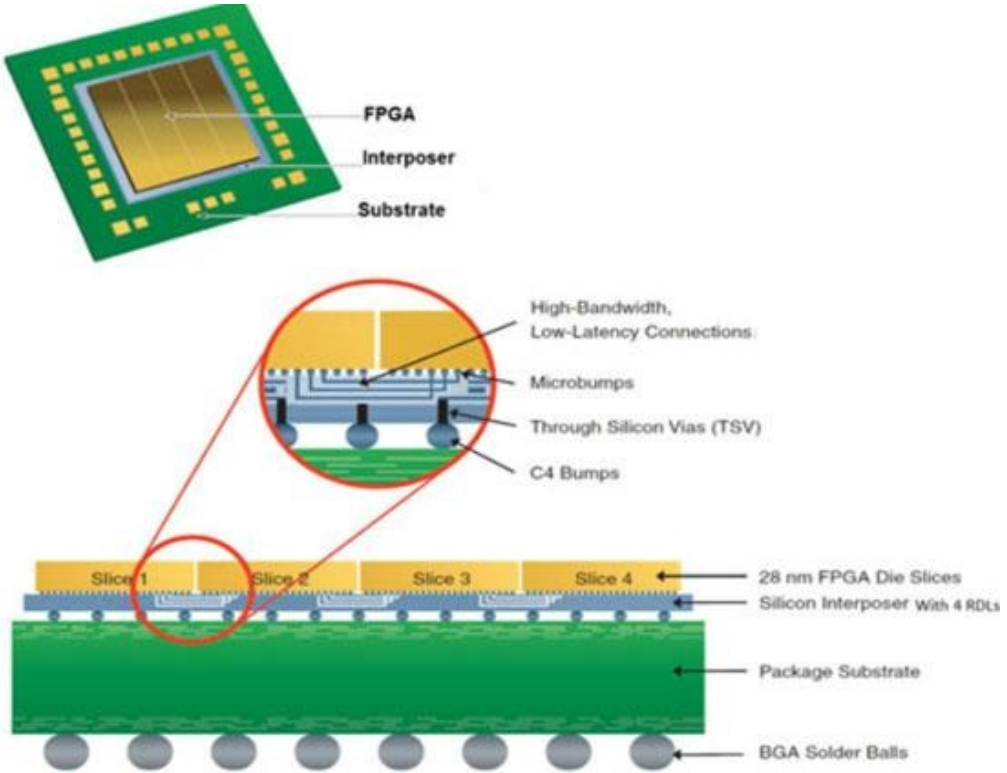
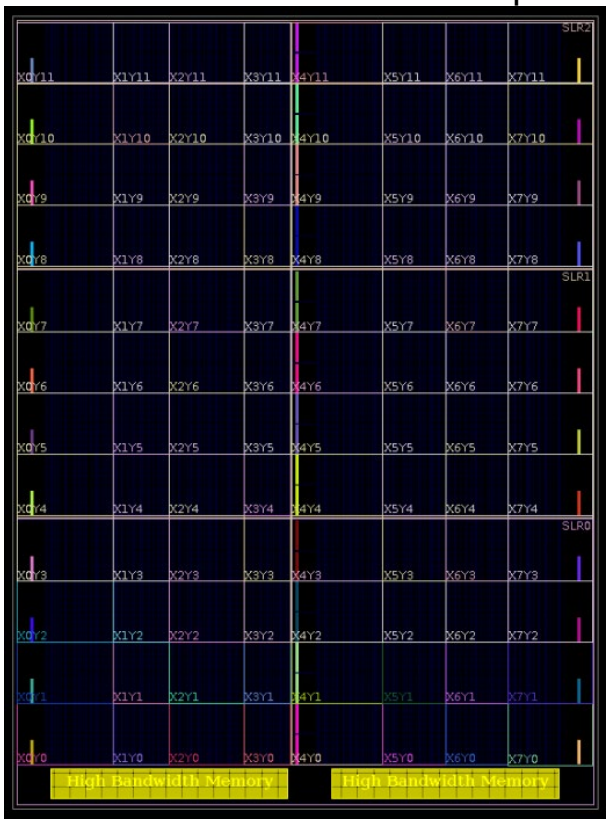
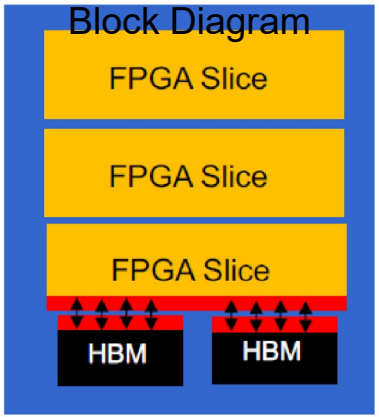
- 3-D Packaging approach
- Combines multiple Super Logic Region (SLR) components mounted on a passive Silicon Interposer.
- SLR contains
  - Input LUTs, Registers, I/O components, Block Memory, DSP blocks, etc…
- Multiple SLR components are stacked next to each other to create the SSI device.

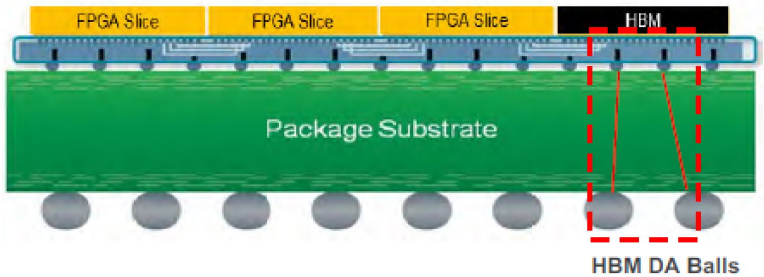


FPGA with HBM

Virtex Ultrascale+ xcvu37p







- **HBM is added as a slice.**
- **SLR0 serves as a master.**
- **HBM comes with DA ports which have to be routed to BGA balls.**

HBM in virtex ultrascale + devices

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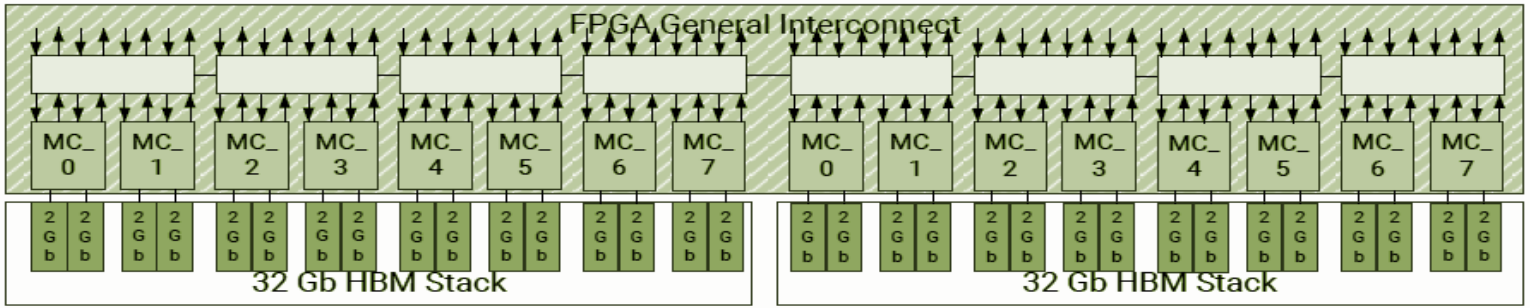
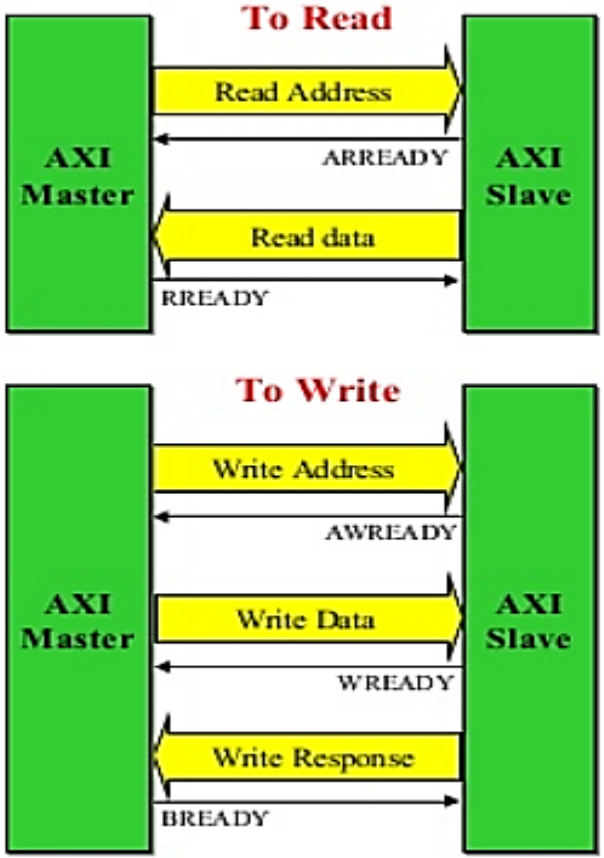


- Divided into two 1024-bit wide HBM stacks.
- Each stack is split into eight independent memory channels.
- Each Memory channels has two 64-bit pseudo channels.
- Each memory channel can be operate at an independent clock rate.
- AXI3 Protocol is used.
- It has a 16 × 16 AXI crossbar switch.

Basic AXI transactiton

- The AXI (Advanced eXtensible Interface) is a point to point interconnect that designed for high performance, high speed microcontroller systems.
- It avoids bus sharing and therefore allow higher bandwidth and lower latency.
- The procedure for the AXI protocol is as follows:
  - Master & slave must “handshake” to confirm valid signals
  - Transmission of control signal must be in separate phases
  - Separate channels for transmission of signals
  - Continuous transfer may be accomplished through burst-type communication



AXI HBM Customize IP – HBM Configuration Selection Tab

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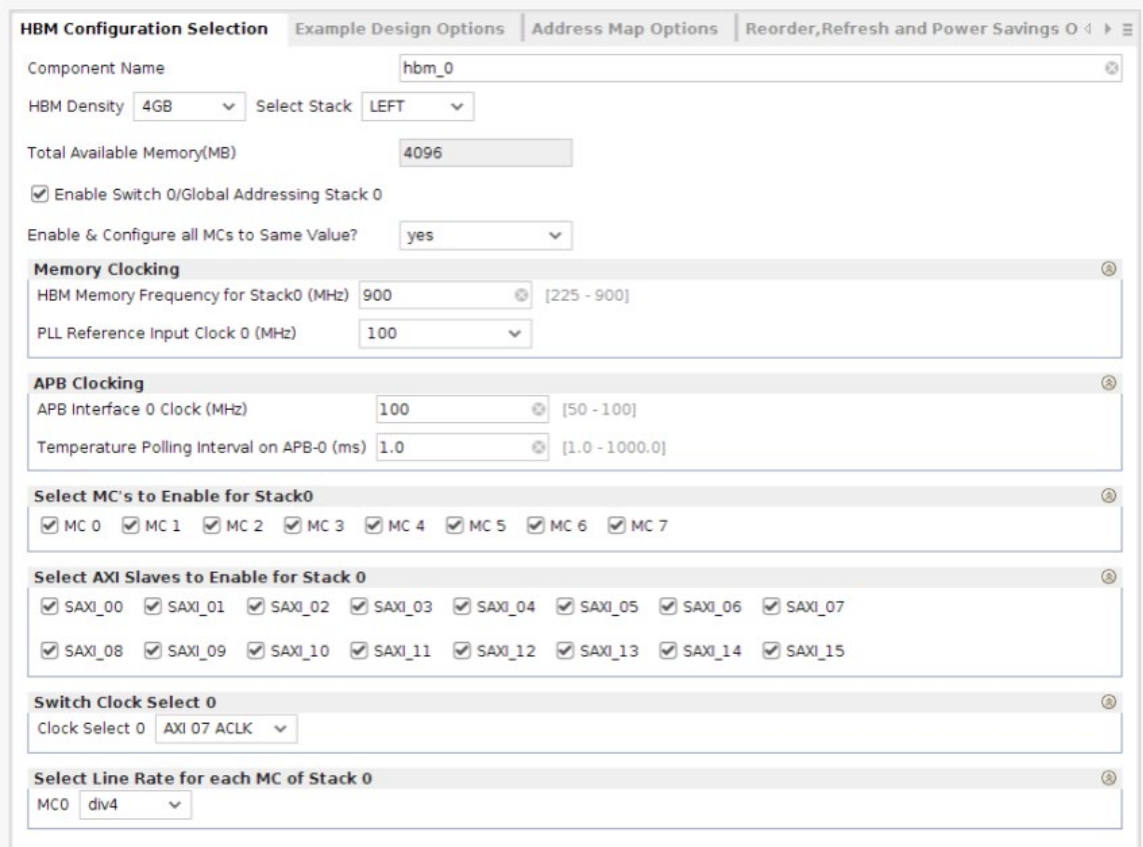

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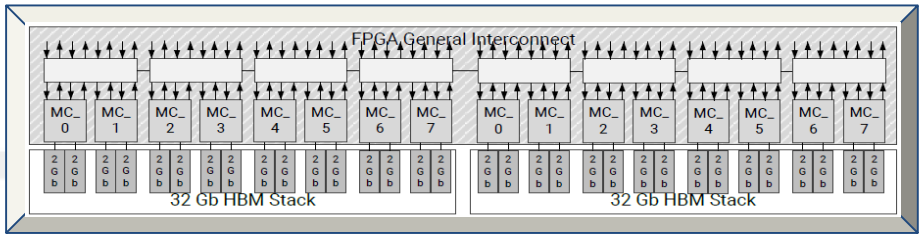

Enable Switch 0/Global Addressing Stack 0

Enable & Configure all MCs to Same Value? yes

Memory Clocking

HBM Memory Frequency for Stack0 (MHz) 900 [225 - 900]

PLL Reference Input Clock 0 (MHz) 100

APB Clocking

APB Interface 0 Clock (MHz) 100 [50 - 100]

Temperature Polling Interval on APB-0 (ms) 1.0 [1.0 - 1000.0]

Select MC's to Enable for Stack0

MC 0 MC 1 MC 2 MC 3 MC 4 MC 5 MC 6 MC 7

Select AXI Slaves to Enable for Stack 0

SAXI_00 SAXI_01 SAXI_02 SAXI_03 SAXI_04 SAXI_05 SAXI_06 SAXI_07

SAXI_08 SAXI_09 SAXI_10 SAXI_11 SAXI_12 SAXI_13 SAXI_14 SAXI_15

Switch Clock Select 0

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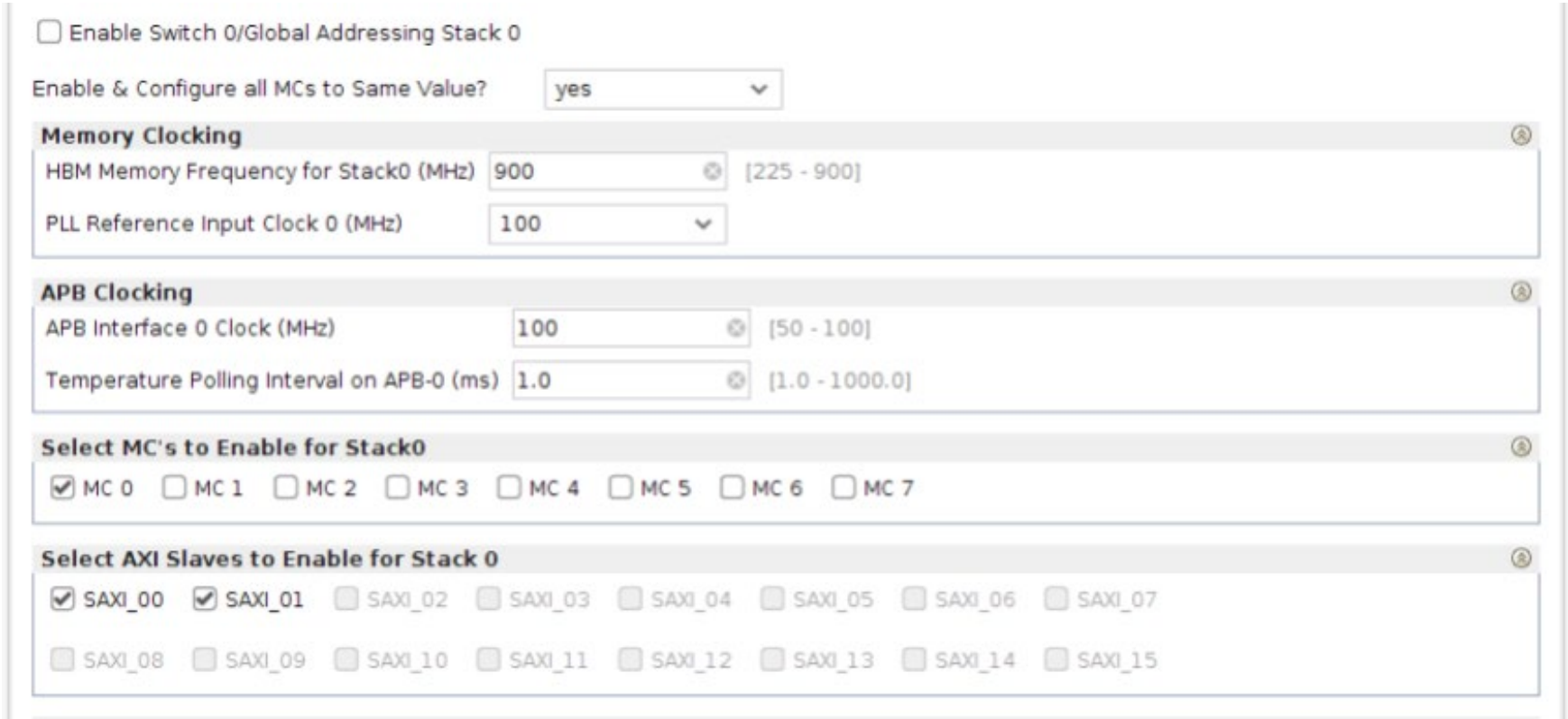

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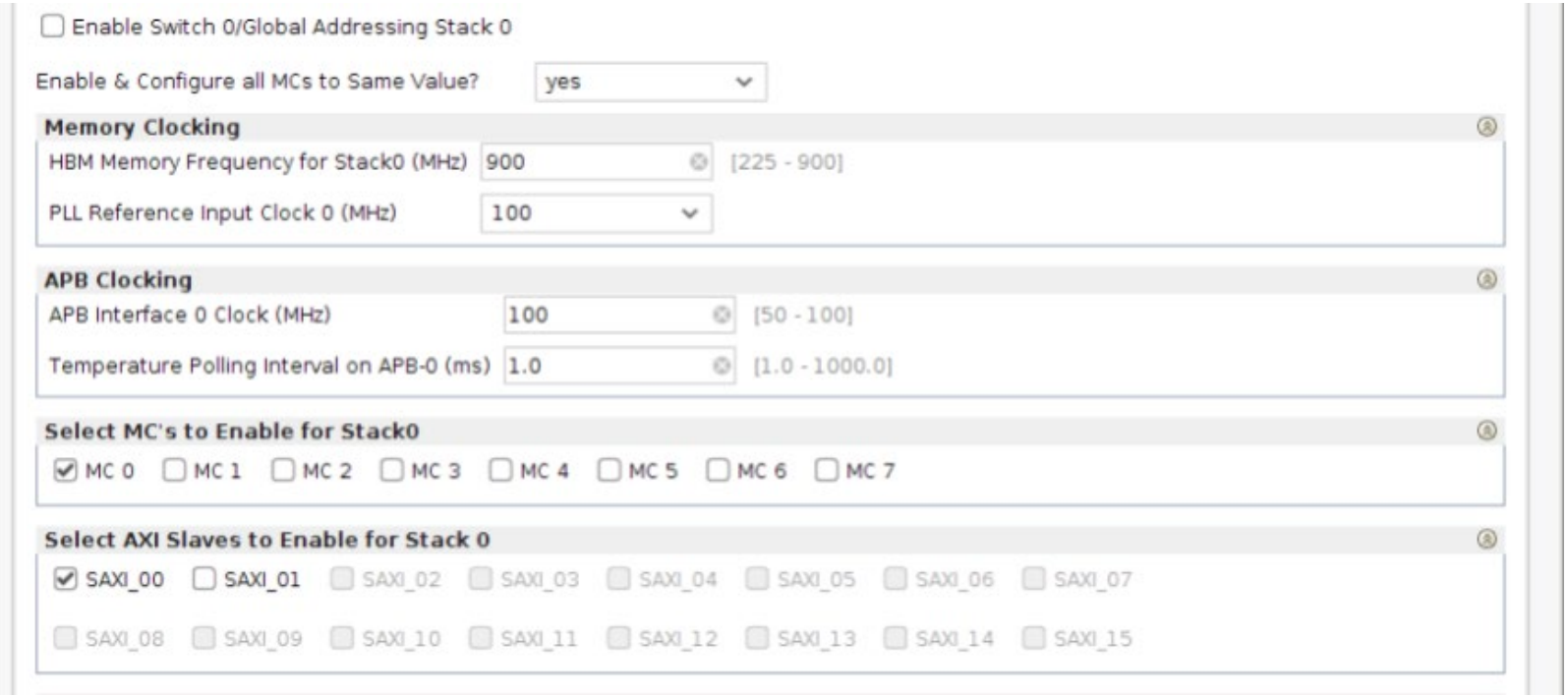

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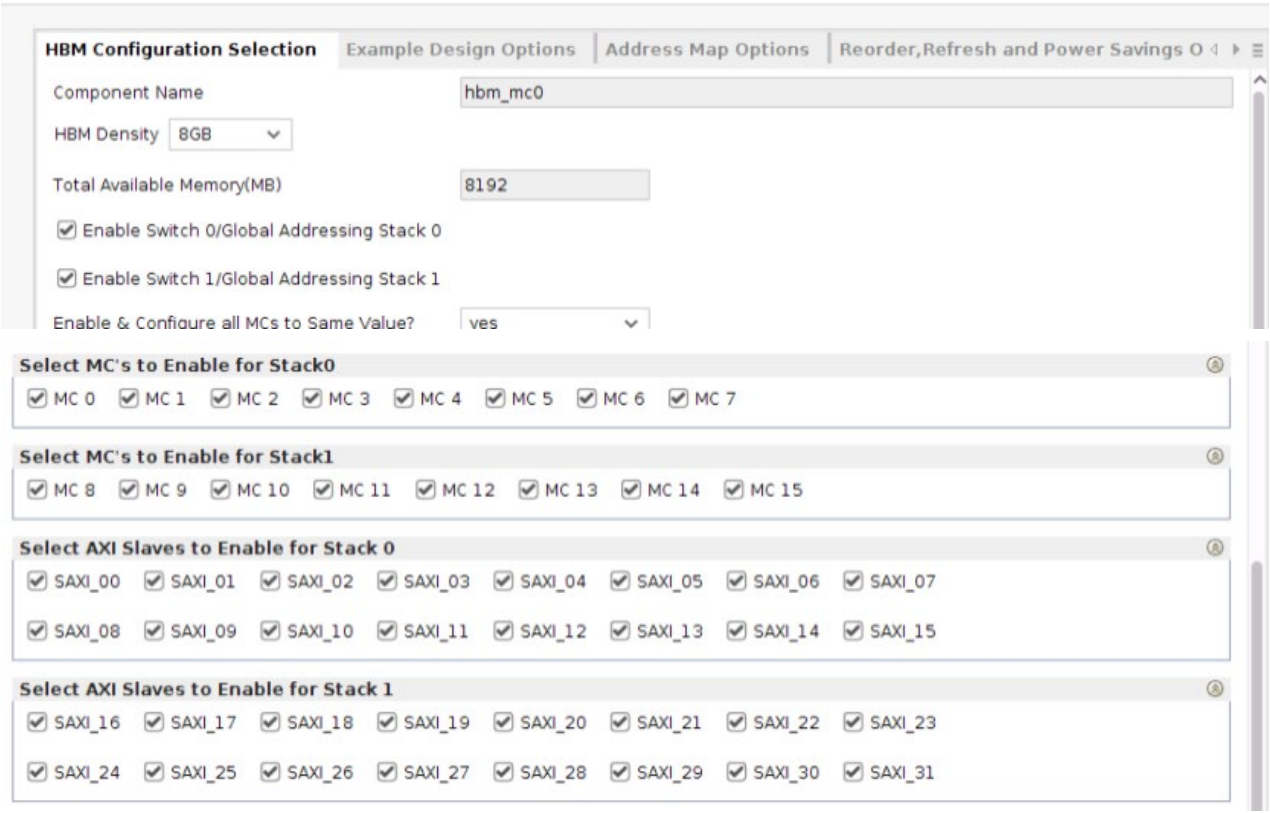

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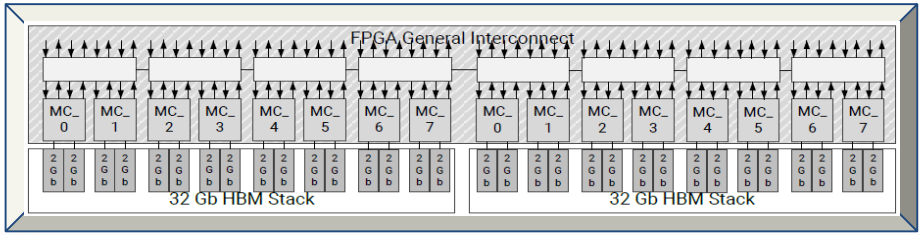

Select MC's to Enable for Stack0

MC 0 MC 1 MC 2 MC 3 MC 4 MC 5 MC 6 MC 7

Select MC's to Enable for Stack1

MC 8 MC 9 MC 10 MC 11 MC 12 MC 13 MC 14 MC 15

Select AXI Slaves to Enable for Stack 0

SAXI_00 SAXI_01 SAXI_02 SAXI_03 SAXI_04 SAXI_05 SAXI_06 SAXI_07

SAXI_08 SAXI_09 SAXI_10 SAXI_11 SAXI_12 SAXI_13 SAXI_14 SAXI_15

Select AXI Slaves to Enable for Stack 1

SAXI_16 SAXI_17 SAXI_18 SAXI_19 SAXI_20 SAXI_21 SAXI_22 SAXI_23

SAXI_24 SAXI_25 SAXI_26 SAXI_27 SAXI_28 SAXI_29 SAXI_30 SAXI_31

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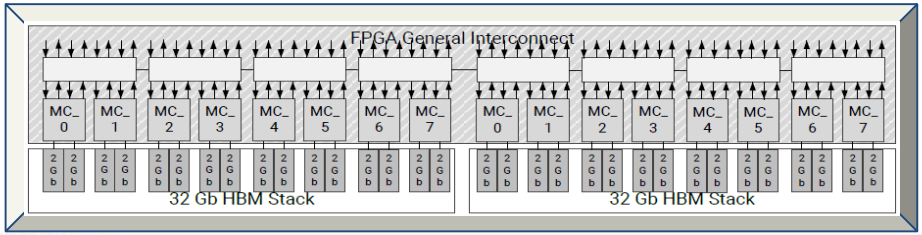

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Select MC's to Enable for Stack1

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Select AXI Slaves to Enable for Stack 0

☑ SAXI_00 ☑ SAXI_01 ☑ SAXI_02 ☑ SAXI_03 ☑ SAXI_04 ☑ SAXI_05 ☑ SAXI_06 ☑ SAXI_07

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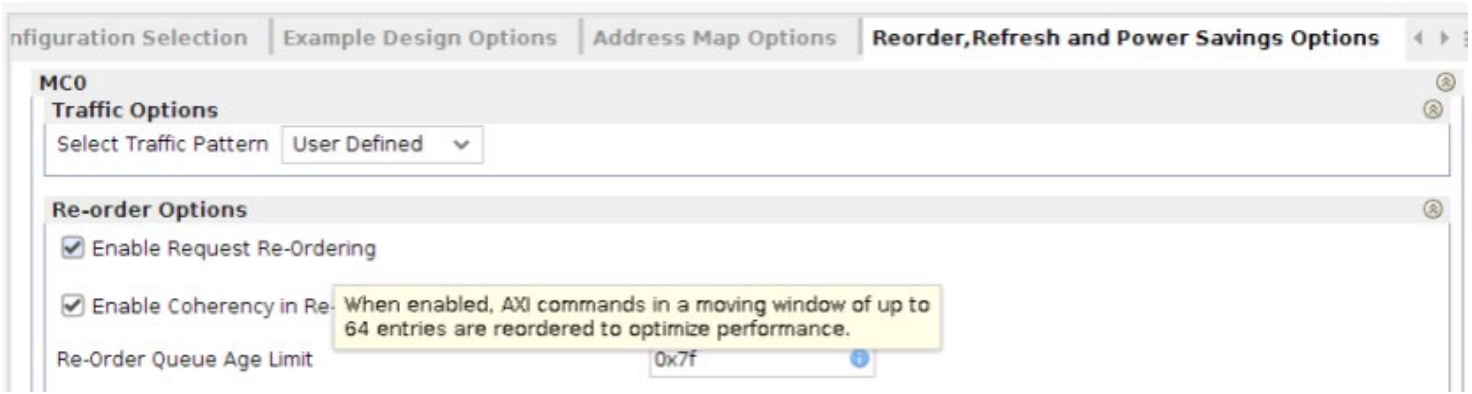
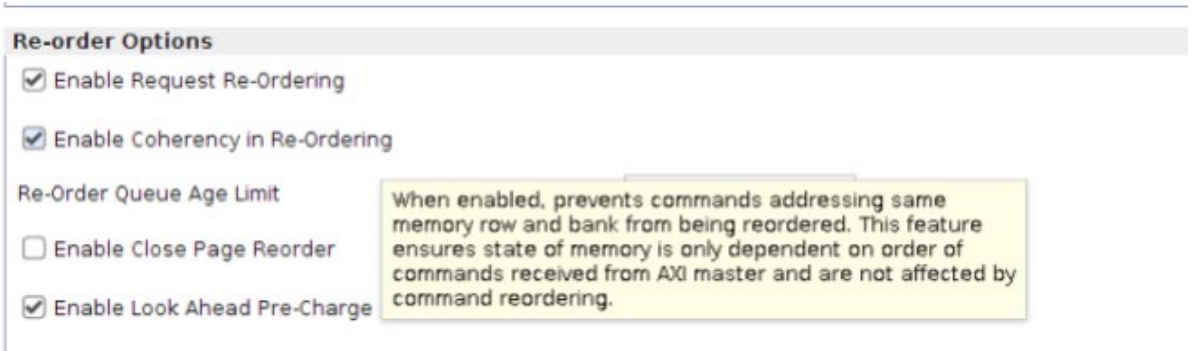
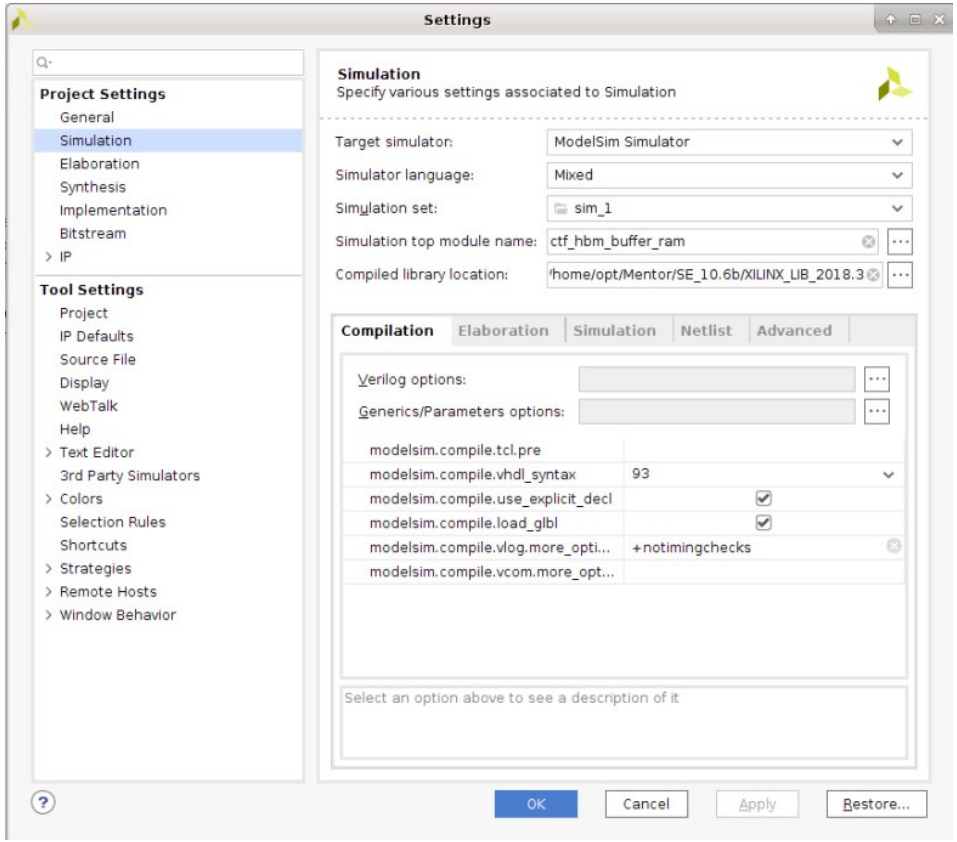




Basic settings required to run the simulation



- **Supported simulators: Modelsim, QuestaSim, IES and Verilog Compiler.**
- **Change the Compiled library location to the location of the compiled library in the installation area.**
- **In the Simulation tab, in the modelsim.simulate.vsim.more_options enter +notimingcheck.**
  - **For Questa simulator, add +notimingchecks in Compilation tab questa.compile.vlog.more_options and in the Simulation tab questa.simulate.vsim.more_options.**
  - **For IES simulator, add -notimingchecks in the Elaboration tab ies.elaboration.ncelab.more_options.**

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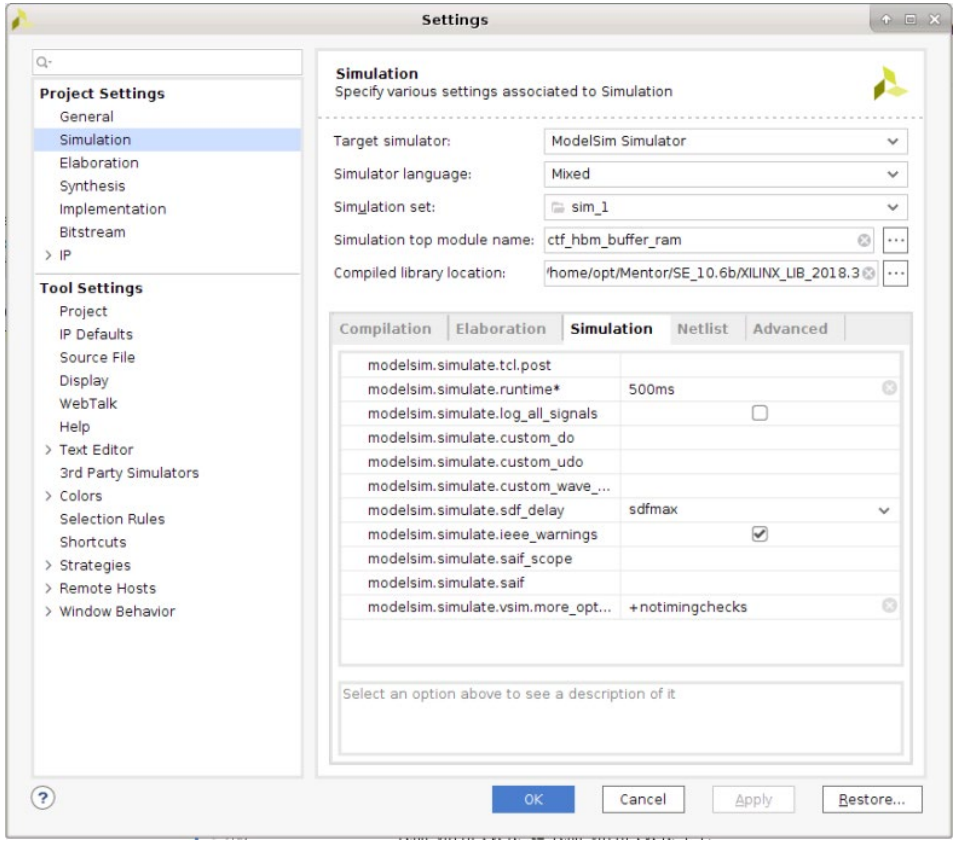

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Performance Measured

(Mco, saxi_00, clk - 450 Mhz)

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Burst Len	Sequential access pattern (read and write)			Sequential write and Random read access pattern
	Throughput (Gbps)	write only Throughput (Gbps)	read only Throughput (Gbps)	Throughput (Gbps)
1	24 (20%) (12Rd + 12Wr)	54 (47%)	54 (47%)	18 (15%) (9Rd + 9Wr)
2	42 (37%) (21 Rd + 21 Wr)	106 (92%)	105 (91%)	24 (20%) (12Rd + 12Wr)
4	50 (43%) (25 Rd + 25 Wr)	107 (93%)	105 (91%)	46 (40%) (23Rd + 23Wr)
8	84 (73%) (42 Rd + 42 Wr)	107.2 (93%)	105 (91%)	80 (69%) (40Rd + 40Wr)
16	106 (92%) (53 Rd + 53 Wr)	107.2 (93%)	105 (91%)	104 (90%) (52Rd + 52Wr)

Simulation result for Sequential access pattern (1MB of data, Burst length = 16)

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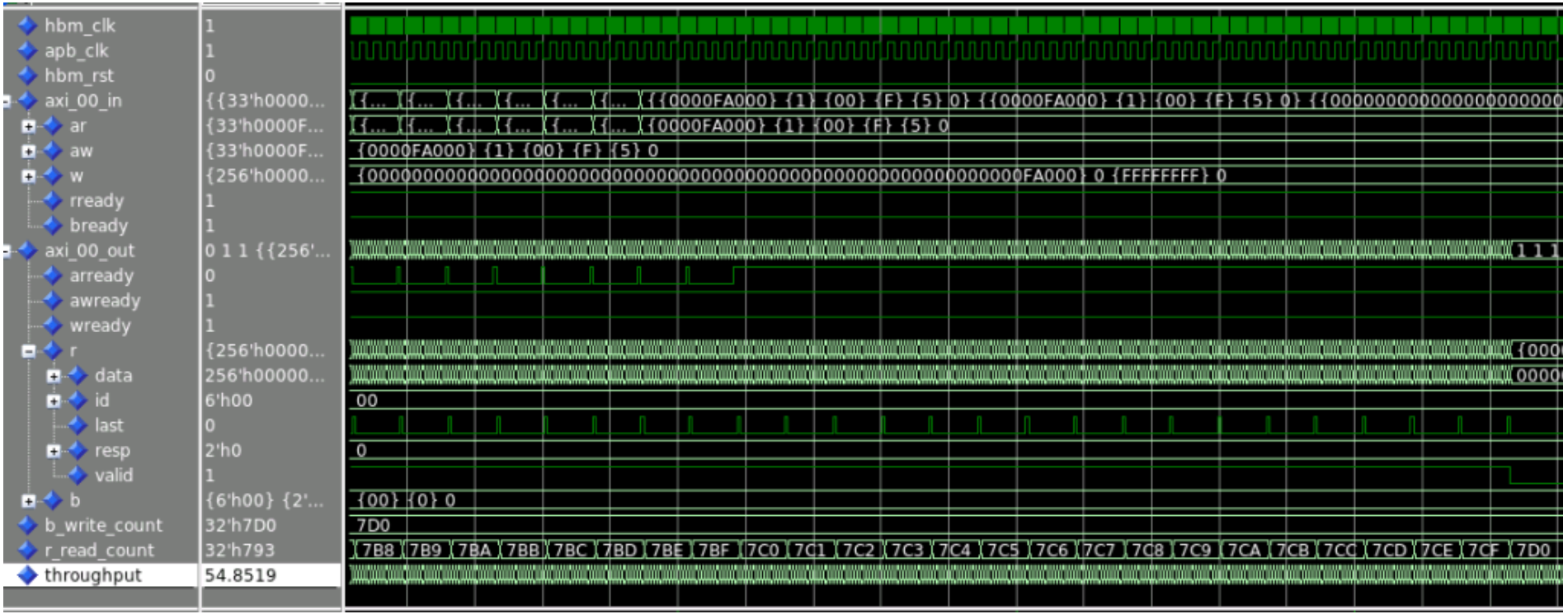
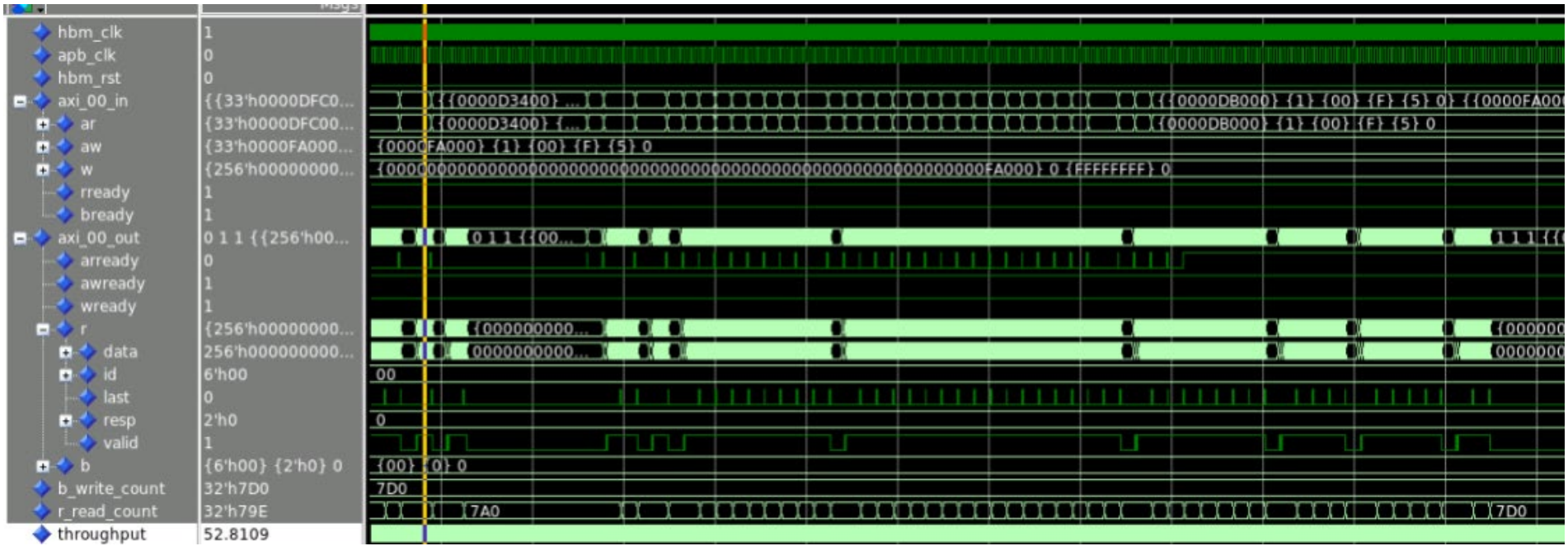


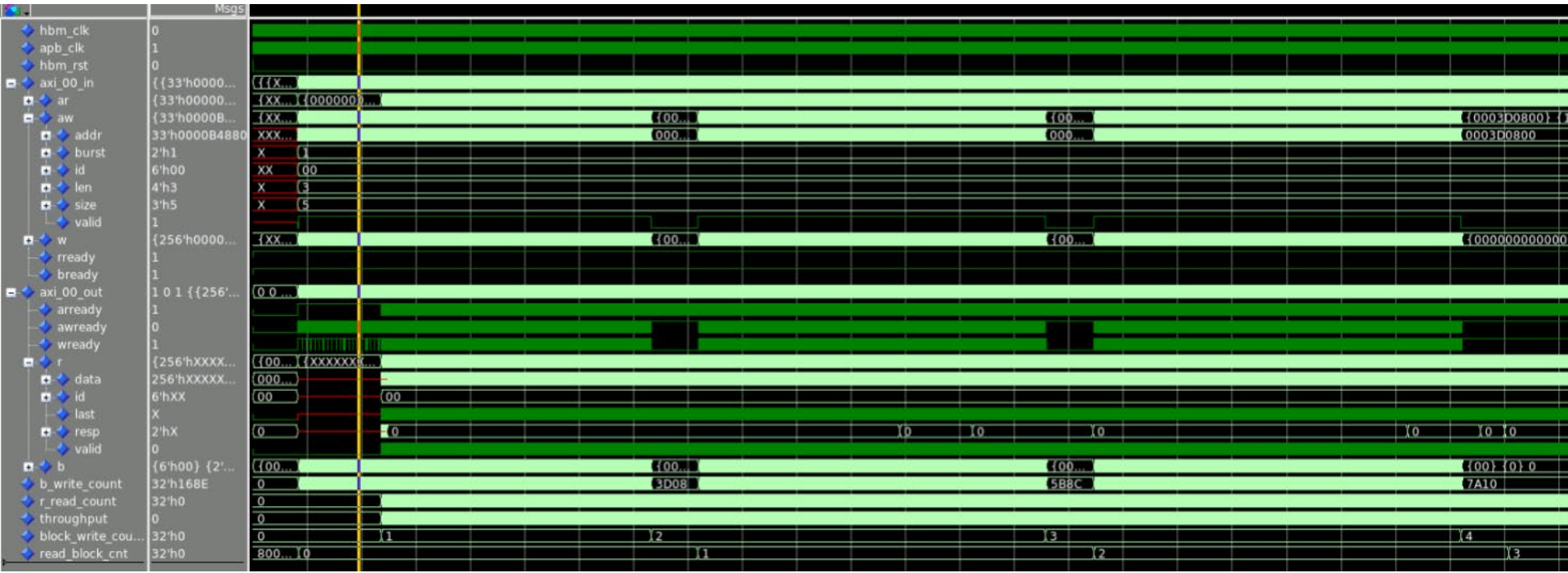
Simulation result for Random read and Sequential write pattern

(1MB of data, Burst length = 16)



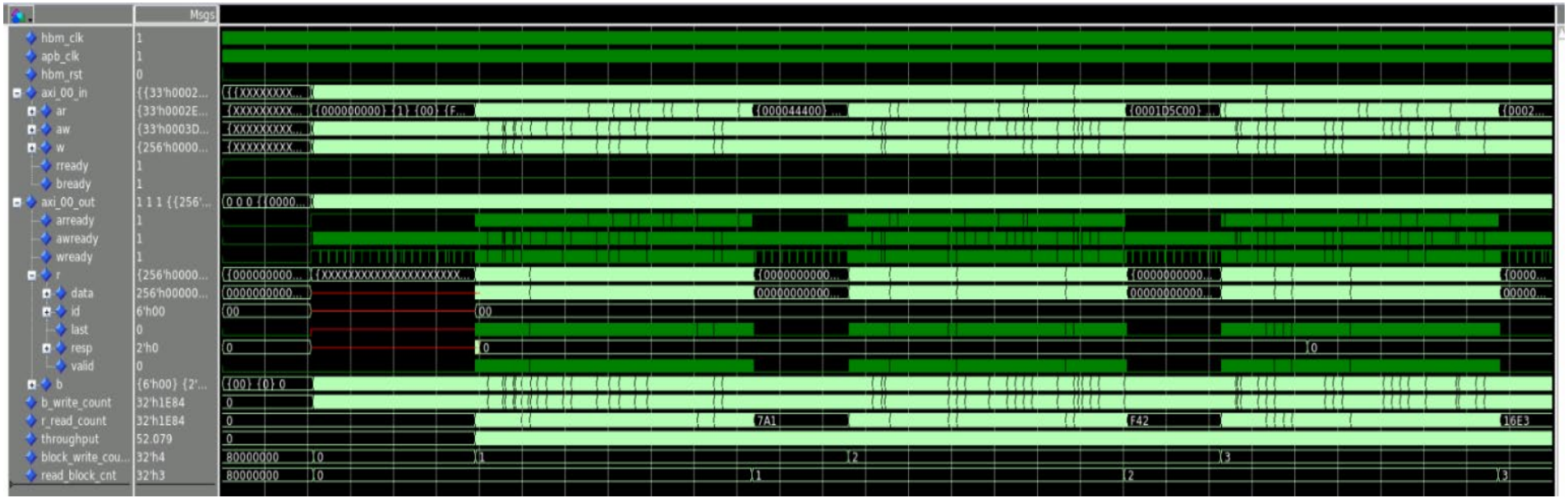
Simulation result for Random read and Sequential write pattern

(Block size = 1MB , Burst length = 4)



Simulation result for Random read and Sequential write pattern

(Block size = 1MB , Burst length = 16)



Questions / Discussion?

Thank-you!